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Figure 1A

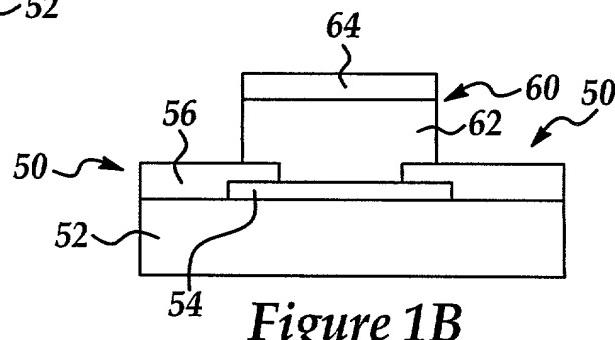


Figure 1B

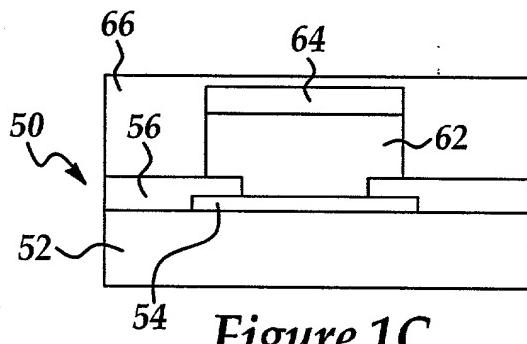


Figure 1C

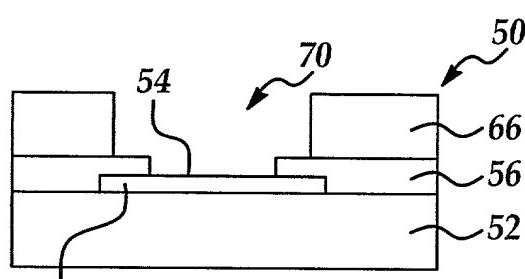


Figure 1E

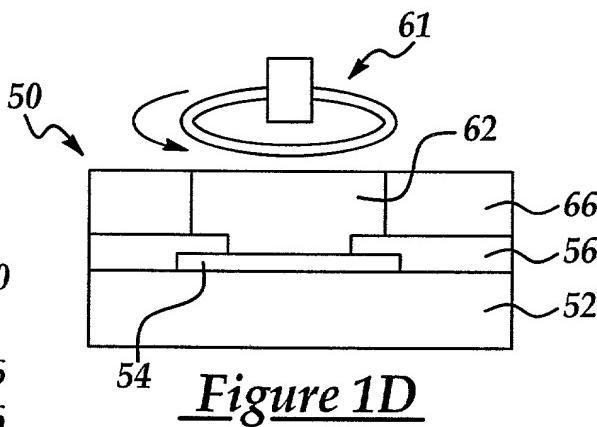


Figure 1D

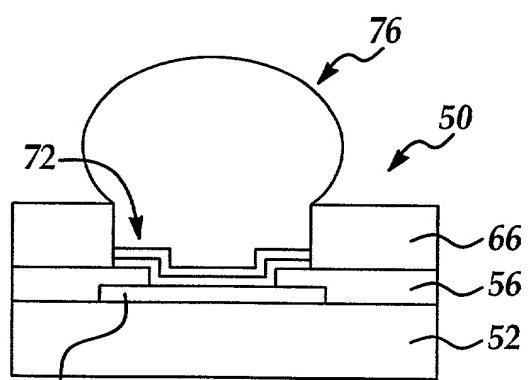


Figure 1E

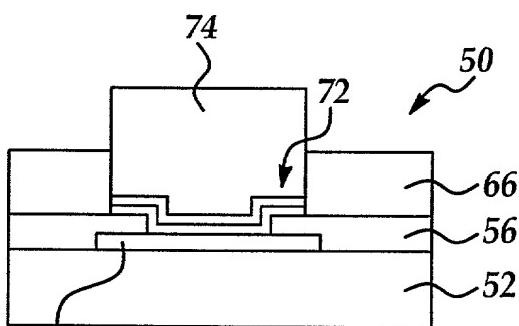


Figure 1F

Inventor(s): Lee
Serial No.: To Be Assigned
Filed: Herewith
For: Method of Making a Wafer Level Chip Scale Package
Attorney Docket No.: 67,200-591

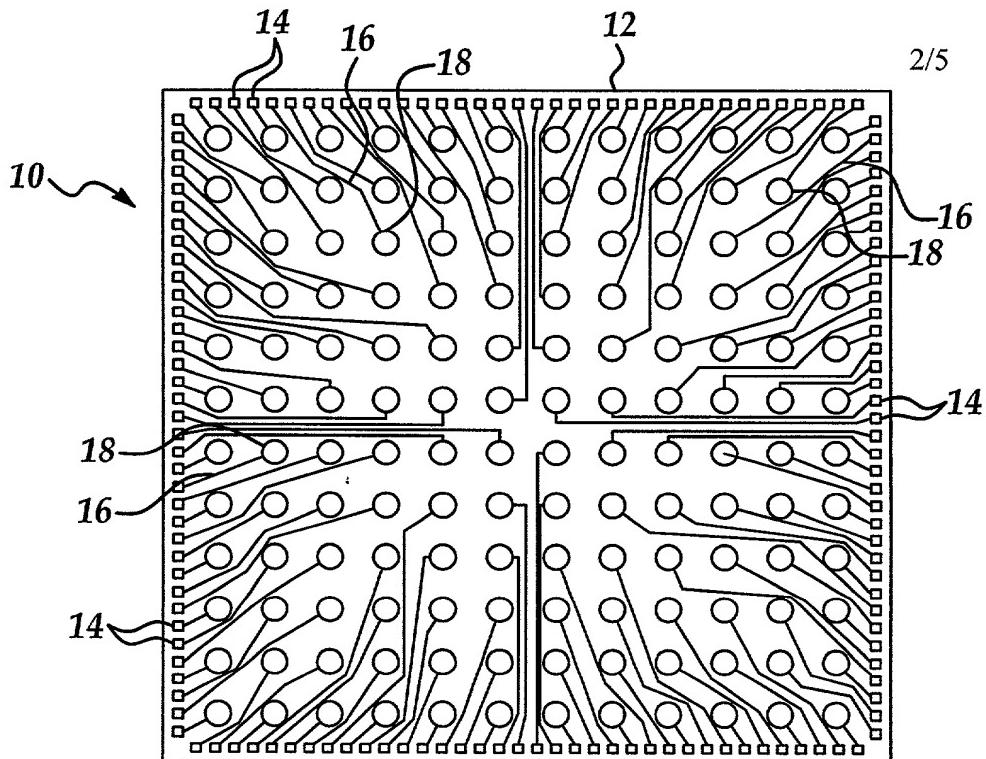


Figure 2
Prior Art

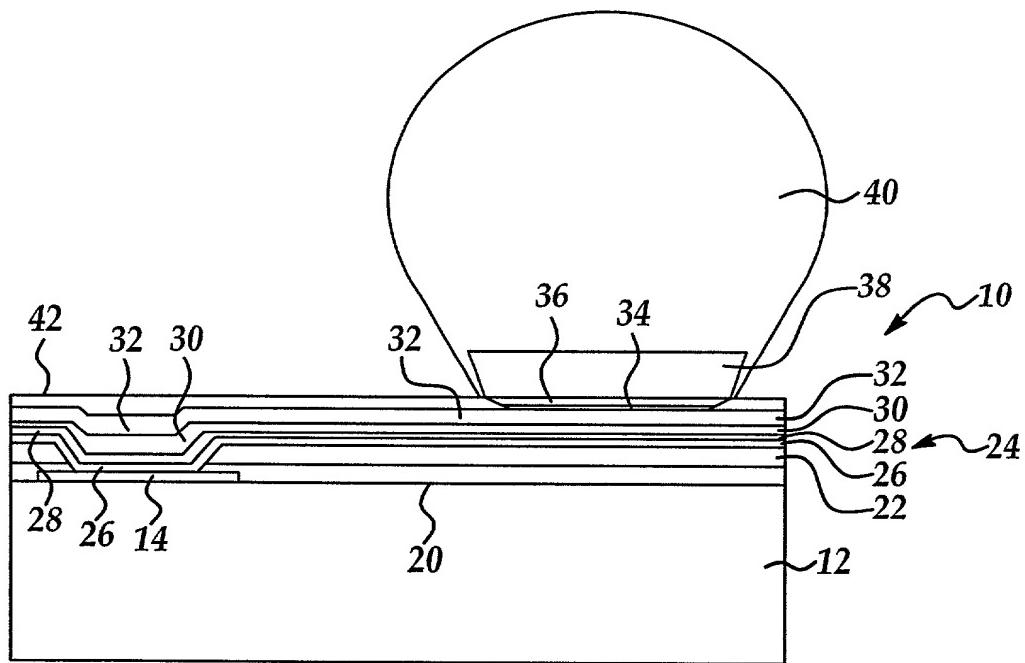


Figure 3
Prior Art

Inventor(s): Lee
Serial No.: To Be Assigned
Filed: Herewith
For: Method of Making a Wafer Level Chip Scale Package
Attorney Docket No.: 67,200-591

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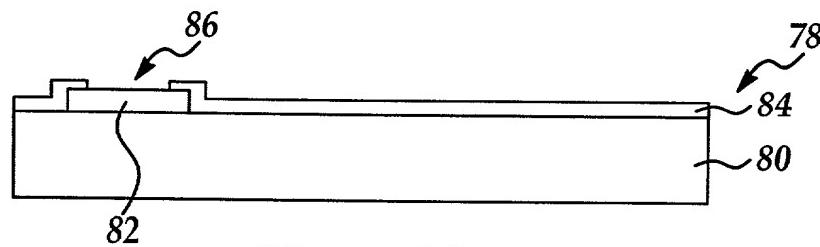


Figure 4A

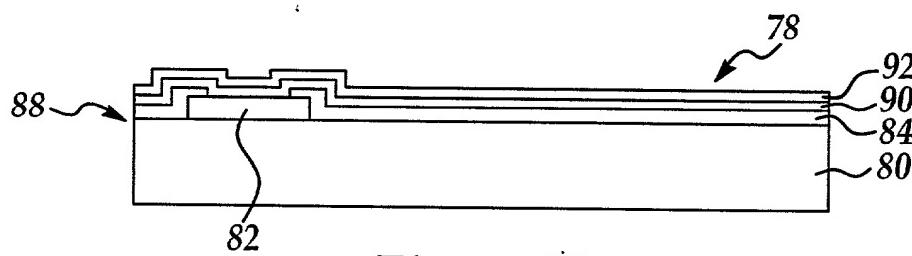


Figure 4B

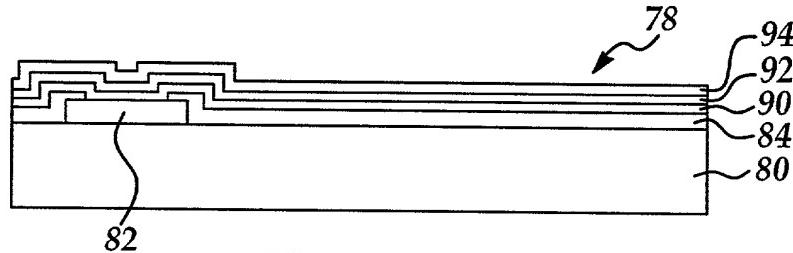


Figure 4C

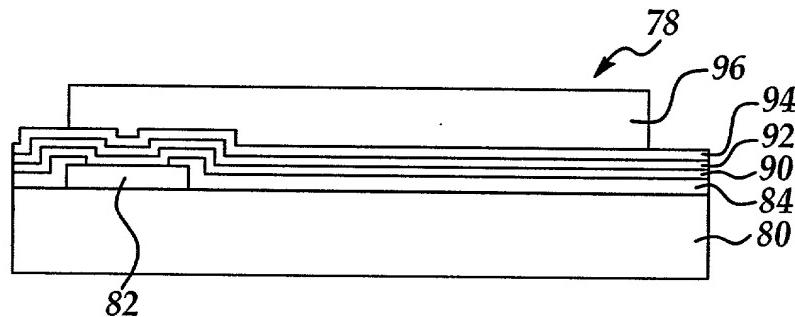


Figure 4D

Inventor(s): Lee
Serial No.: To Be Assigned
Filed: Herewith
For: Method of Making a Wafer Level Chip Scale Package
Attorney Docket No.: 67,200-591

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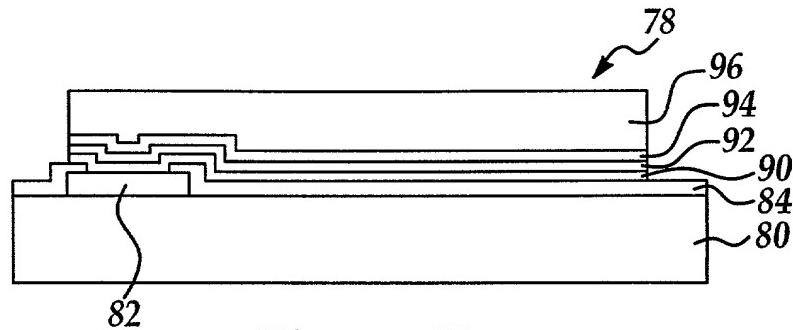


Figure 4E

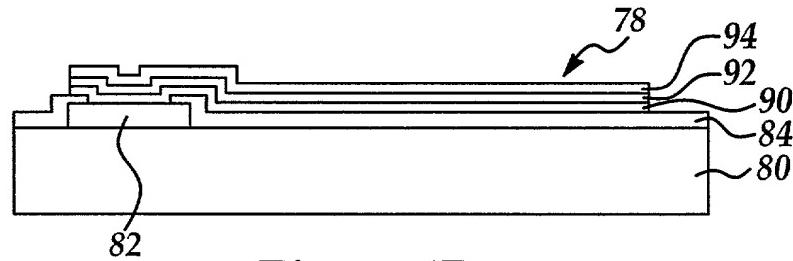


Figure 4F

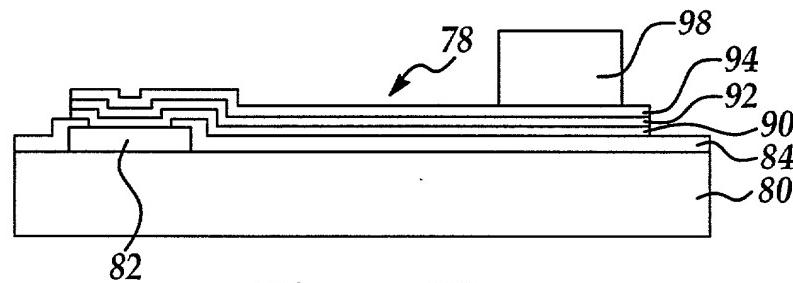


Figure 4G

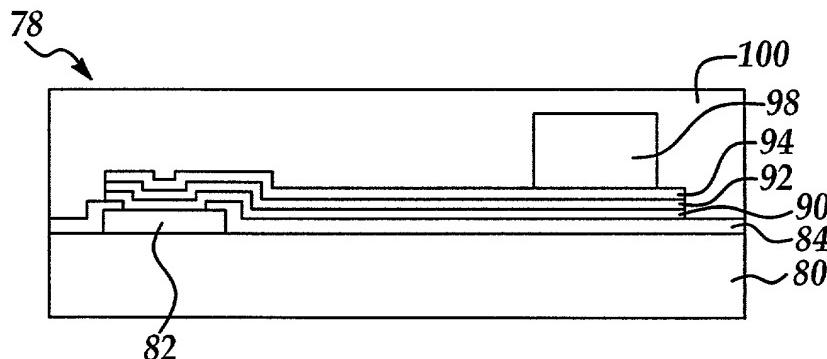


Figure 4H

Inventor(s): Lee
Serial No.: To Be Assigned
Filed: Herewith
For: Method of Making a Wafer Level Chip Scale Package
Attorney Docket No.: 67,200-591

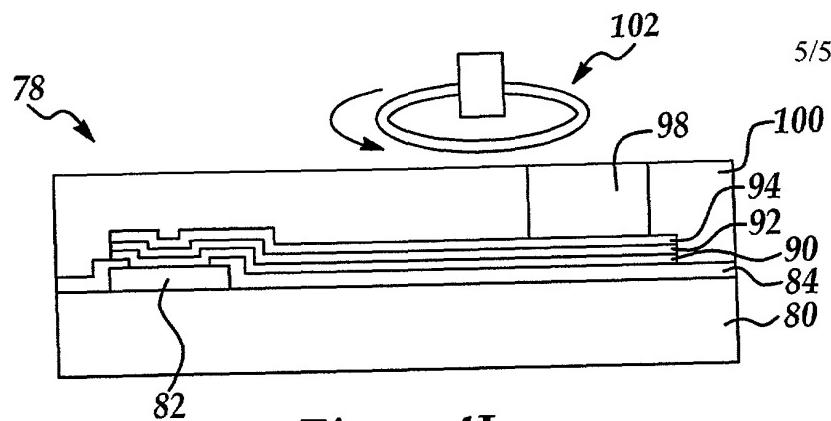


Figure 4I

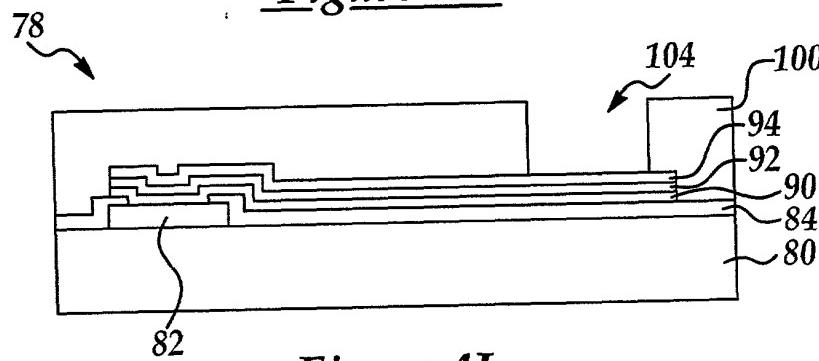


Figure 4J

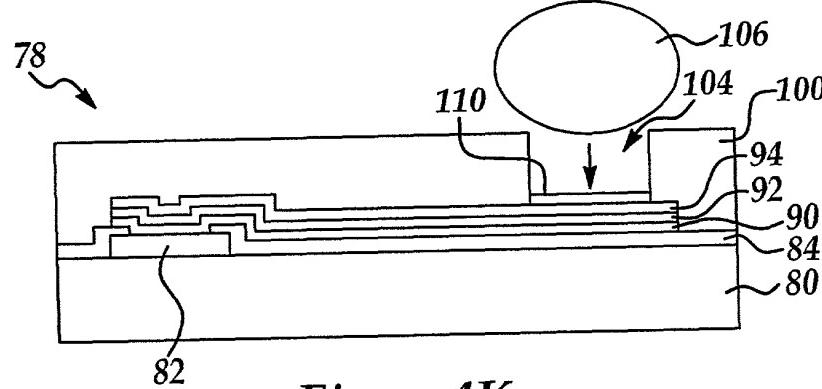


Figure 4K

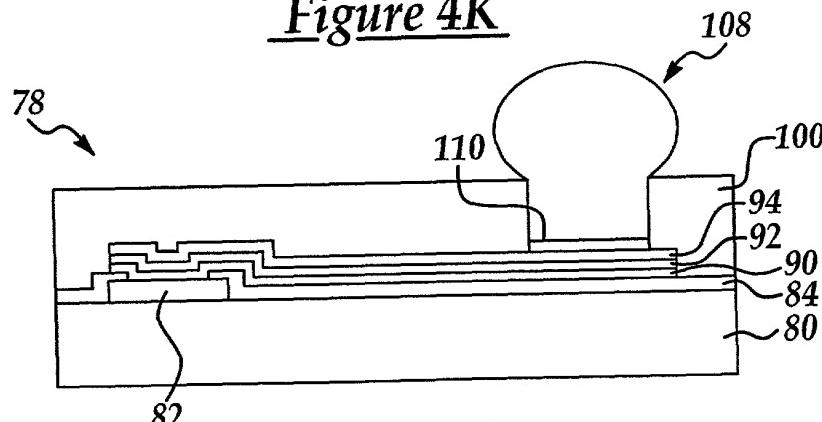


Figure 4L